REMARKS/ARGUMENTS

Reconsideration of the application is requested.

Claims 1-4, and 6-11 remain in the application. Claims 1, 3, and 6-10 have been amended. Claims 5 and 12 have been cancelled. Claims 10-11 have been previously withdrawn and rejoinder of claims 10-11 has been requested.

In item 2 on pages 2-5 of the above-mentioned Office action, claims 1-4, 6, and 8 have been rejected as being anticipated by Cho (US Pat. No. 6,087,718) under 35 U.S.C. § 102(e).

In item 3 on pages 5-8 of the above-mentioned Office action, claims 1-4 and 6-9 have been rejected as being anticipated by Chang et al. (US Pat. No. 6,483,181 B2) under 35 U.S.C. § 102(e).

In item 4 on page 8 of the above-mentioned Office action, claims 7 and 9 have been rejected as being unpatentable over Cho in view of Chang et al. under 35 U.S.C. § 103(a).

In item 5 on page 9 of the above-mentioned Office action, claim 5 has been rejected as being unpatentable over Cho in view of DE 100 03 670 A1 under 35 U.S.C. § 103(a).

In item 6 on pages 9-10 of the above-mentioned Office action, claim 5 has been rejected as being unpatentable over Chang et al. in view of DE 100 03 670 A1 under 35 U.S.C. § 103(a).

The rejections have been noted and claim 1 has been amended in an effort to even more clearly define the invention of the instant application. Support for the changes is found in original claim 5.

Before discussing the prior art in detail, it is believed that a brief review of the invention as claimed, would be helpful.

Claim 1 calls for, inter alia:

> a first interposer layer or interposer film configured on said active surface of said first semiconductor chip, said first interposer layer or interposer film having first bonding fingers, first interposer lines and first bonding surfaces; and
>
> a second interposer layer or interposer film configured on said active surface of said second semiconductor chip, said second interposer layer or interposer film having second bonding fingers, second interposer lines and second bonding surfaces;
>
> each one of said plurality of first bonding connections connecting one of said first bonding surfaces on said first interposer layer or interposer film to said inner section of one of said plurality of flat conductors; and
>
> each one of said plurality of second bonding connections connecting one of said second bonding surfaces on said second interposer layer or interposer film to said transitional section of one of said plurality of flat conductors.

The prior art fails to teach a stacked electronic component which includes an interposer layer or film disposed on the active surface of each chip and in which the interposer is bonded to flat conductors which form the external contacts to the package.

The invention of the instant application addresses the object of providing a more reliable stacked electronic component and in particular, addresses the object of the reliable testing of semiconductor chips before the chips are mounted in the stack. The contact pads positioned on the active surface of the semiconductor chip are extremely small and, therefore, it is difficult to test the functionality of the chip before it is mounted in the stack. This leads to wastage, particularly, in the stacked component since it is often difficult or impossible to remove a defective chip which is already mounted in the stack. Alternatively, the whole stack including correctly functioning chips has to be discarded along with the defective chip.

The invention of the instant application avoids the problem by providing an electronic component in which an interposer is disposed on the active surface of each chip of the stack. The interposer has bonding fingers which are connected to the chip

contact pads and contact lines leading outwards to bonding areas which are of a larger size. The chip can, therefore, be tested by positioning contact probes on these larger areas. The interposer layer also provides a cushioning effect to protect the surface of the chip from the pressure exerted by the contact probes. Correctly functioning chips are then mounted in a stack in which flat conductors are positioned between the two chips. The first chip is bonded to the inner portions of the flat conductors and the second chip to the transitional portion of the flat conductor. This enables a simple stacking of chips which have the same chip contact pad layout and avoids the use of chips with a mirror pad arrangement and the use of complex rewiring layers or bonding arrangements.

The provision of a stacked electronic component in which the rewiring structure includes an interposer layer and flat conductors is not obvious from the cited prior art references. The cited prior art references give a person skilled in the art no reason to provide a leadframe-type electronic component which also includes an interposer layer on the active surface of the chip to provide a first stage of the rewiring structure. Conventionally, as taught by DE 100 03 670 A1, the interposer layer provides the rewiring structure from the chip contact pad directly to the outer contact of the package. The

prior art gives a person skilled in the art no reason to provide a semiconductor chip which includes an interposer layer that provides only a part of the rewiring structure. Similarly, the prior art gives a person skilled in the art no reason to provide a stacked electronic component in which only the intermediate and outer portion of the rewiring structure is provided by flat conductors.

It is accordingly believed to be clear that none of the references, whether taken alone or in any combination, either show or suggest the features of claim 1. Claim 1 is, therefore, believed to be patentable over the art and since claims 2-4 and 6-9 are dependent on claim 1, they are believed to be patentable as well. Claim 5 has been cancelled.

In view of the foregoing, reconsideration and allowance of claims 1-4 and 6-9 are solicited. Rejoinder of method claims 10-11 is requested upon allowance of product claims under MPEP 821.04 ("if applicant elects claims directed to the product, and a product claim is subsequently found allowable, withdrawn process claims which depend from or otherwise include all the limitations of the allowable product claim will be rejoined").

In the event the Examiner should still find any of the claims to be unpatentable, counsel would appreciate a telephone call so that, if possible, patentable language can be worked out.

If an extension of time for this paper is required, petition for extension is herewith made. Please charge any fees which might be due with respect to 37 CFR Sections 1.16 and 1.17 to the Deposit Account of Lerner and Greenberg, P.A., No. 12-1099.

Respectfully submitted,

Yonghong Chen
Reg. No. 56,150

Yonghong Chen
For Applicants

YC

December 30, 2004

Lerner and Greenberg, P.A.
Post Office Box 2480
Hollywood, FL 33022-2480
Tel: (954) 925-1100
Fax: (954) 925-1101